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09/863,888	05/22/2001	Anthony William Jorgenson	KES-00-001	9420

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EXAMINER	
JUNTIMA, NITTAYA	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/863,888	JORGENSON ET AL.	
	Examiner	Art Unit	
	Nittaya Juntima	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) *4,7,8,15,18-21,26,28-36,38,40-44 and 46-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,5,9-12,16,25,27,37,39,45,49-54 and 57-70* is/are rejected.

7)☒ Claim(s) *2,3,6,13,14,17,22-24,55 and 56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on 9/12/2005.

2. Claims 4, 7-8, 15, 18-21, 26, 28-36, 38, 40-44, and 46-48 have been cancelled.

3. Claims 1, 12, 25, 37, 45, 49-54, 57-58, 60-65, and 67-70 are presently rejected under 35 U.S.C. 102(e).

4. Claims 5, 9-11, 16, 27, 39, 59 and 66 are presently rejected under 35 U.S.C. 103(a).

5. Claims 2-3, 6, 13-14, 17, 22-24, and 55-56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Specification

6. The disclosure is objected to because of the following informalities:

- on page 1, line 20, please provide the provisional patent application number,
- on page 9, line 27, please provide the status (e.g. abandoned) of the cited application;
- on page 14, line 18, "pending" should be changed to "a provisional patent"

  line 18, please provide the provisional patent application number;
- on page 16, line 31, please provide the application number and status of the cited application;
- on page 11, line 27-29, please verify why the clock signal is divided by ten as stated and shown in Fig. 3, element 330 of the drawing as it is unclear how the data would be read out

of the elastic store 350 to meet the output clock rate of unit 360 at 155.52 MHz when the data is being written into the elastic store 350 at a clock rate of one hundredth of the data rate (clock signal has a rate of one tenth of the data rate of the encoded data, page 8, lines 4-6).

Appropriate correction is required.

Claim Objections

7. Claims 1, 9-10, 25, 37, 39, 57, 59, 60, and 64 are objected to because of the following informalities:

- in claim 1, lines 5 and 6, "multiplexing" and "multiplexed" should be changed to "inverse multiplexing" and "inverse multiplexed," respectively, since the received data as shown in the corresponding embodiment of Fig. 1 (see claims 9-11) includes 9-bit data which is to be inverse multiplexed (i.e. demultiplexed) by unit 130 in order to output eight STS-3s (note that inverse multiplex is not the same as multiplex);

- in claim 9, lines 1 and 2, "multiplexing" and "multiplexed" should be changed to "inverse multiplexing" and "inverse multiplexed," respectively;

- in claim 10, line 1, "multiplexed" should be changed to "inverse multiplexed;"

- in claim 25, line 5, "demultiplexer" and "demultiplex" should be changed to "multiplexer" and "multiplex," respectively, since the received data as shown in the corresponding embodiment of Fig. 2 includes eight frame aligned STS-3 signals which are to be multiplexed/combined by unit 220 in order to output 9-bit data (note that demultiplex means to separate two or more signals previously combined by compatible multiplexing equipment);

- in claim 37, line 4, "demultiplexing" should be changed to "multiplexing," and

line 5, "demultiplexed" should be changed to "multiplexed" for the same reason above;

- in claim 39, line 1, "38" should be changed to "37;"

- in claim 57, lines 2-3 and 5, "demultiplexer," "demultiplex," and "demultiplexed" should be changed to "multiplexer," "multiplex," and "multiplexed," respectively, since the received data as shown in corresponding Fig. 2 (see claim 58) includes eight frame aligned STS-3 signals which contain 9-bit data and are to be multiplexed/combined by unit 220 in order to output 9-bit data (note that demultiplex means to separate two or more signals previously combined by compatible multiplexing equipment, therefore, it is technically incorrect to demultiplex the incoming 9-bit data and obtain 9-bit data);

- in claim 59, line 1, "demultiplexer" should be changed to "multiplexer;"

- in claims 60 and 61, line 3, "multiplex" should be changed to "demultiplex" to correctly represent the corresponding embodiment shown in Fig. 4;

- in claim 64, lines 2 and 4, "demultiplexing," and "demultiplexed" should be changed to "multiplexing" and "multiplexed," respectively, since the received data as shown in corresponding Fig. 2 (see claim 65) includes eight frame aligned STS-3 signals which contain 9-bit data and are to be multiplexed/combined by unit 220 in order to output 9-bit data (note that demultiplexing means to separating two or more signals previously combined by compatible multiplexing equipment, therefore, it is technically incorrect to demultiplex the incoming 9-bit data and obtain 9-bit data).

Appropriate correction is required.

8. The indicated allowable subject matter in the previous Office action is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Stanger et al. ("Stanger") (USPN 6,097,435).

Regarding claims 1 and 12, as shown in Fig. 4, Stanger teaches an apparatus comprising:

A clock recovery unit (an input buffer 70) for receiving an encoded data (encoded data processed by an encoder 26 in Fig. 3 is received at an input buffer 70, col. 4, lines 32-40).

A data translation unit (a depacketizer 72) for mapping said received data to a predetermined data (encoded data is depacketized by a depacketizer 72, col. 4, lines 40-43).

An inverse multiplexer for inverse multiplexing said mapped predetermined data (the depacketized data is demultiplexed by a demultiplexer 74, col. 4, lines 40-43).

Wherein the clock recovery unit is to detect a data rate of said received encoded data (the input buffer 70 determines the data rate of the encoded data, col. 4, lines 32-37).

11. Claims 25, 37, and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Rowan et al. ("Rowan") (USPN 6,529,303 B1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 25 and 37, as illustrated in Fig. 5A, Rowan teaches an apparatus comprising:

A plurality of FIFOs (526 for receiving and synchronize the four byte-wide parallel TS-3 signals) each configured to frame align a corresponding one of a plurality of STS-3 signals (col. 13, lines 24-30).

A multiplexer (524) configured to multiplex received data including said frame aligned STS-3 signals (col. 13, lines 30-33).

A data translation unit coupled to the multiplexer configured to translate the multiplexed data to a predetermined data (a unit inherently included in 522 that adds STS-12 framing to complete the STS-12 signal, col. 13, lines 33-35).

A serializer coupled to said data translation unit configured to receive said translated predetermined data and accordingly to generate a corresponding encoded data (another unit inherently included in 522 that must receive the complete STS-12 signal and convert the signal from byte-wide parallel to serial, col. 13, lines 33-35).

Regarding claim 45, it is inherent that the step of synchronizing the translated predetermined data (converted STS-12 signal from byte-wide parallel to serial) must be included

in order for the converted STS-12 signal to produce the data rate of STS-12 with clock PLL by the parallel to serial converter 522, Fig. 5A and further converted into the outgoing OC-12 tributary 160A, col. 13, lines 33-37.

12. Claims 49-50, 57-58, 60-65, and 67-70 are rejected under 35 U.S.C. 102(e) as being anticipated by Azizoglu et al. ("Azizoglu") (USPN 6,430,201 B1).

Regarding claim 49, as shown in Fig. 2, Azizoglu teaches a method comprising :

Receiving an encoded data (unit 22-1 receives 8B/10B encoded data, col. 4, lines 39-44).

Mapping said received data to a predetermined data, wherein said predetermined data includes a 9-bit data (the 10-bit parallel stream is decoded by codec 2201 to output an 8 bit-parallel stream with a ninth bit added, col. 4, lines 42-51).

Multiplexing said mapped predetermined data (the stream is then supplied to the multiplexing and framing logic 26, col. 4, lines 55-62).

Regarding claim 50, it is inherent that said 9-bit data includes one of an arbitrary set of 9-bit data (col. 4, lines 47-51 and 53-55).

Regarding claims 57 and 64, as illustrated in Fig. 4, Azizoglu teaches an apparatus comprising:

A multiplexer (MUX) configured to multiplex received data, wherein said multiplexed data includes a 9-bit data (at the receiving side, the received data containing a 9-bit data, i.e. an 8-bit parallel stream with a ninth bit added transmitted from the transmitting side in Fig 2, col. 4, lines 39-44 and 47-51, must be received and multiplexed by MUX then transmitted to a codec 22-1, col. 6, lines 4-14).

A data translation unit (codec 8B/10B 22-1) coupled to the multiplexer (MUX) configured to translate the multiplexed data to a predetermined data (codec 22-1 re-insert the run-length code, col. 6, lines 12-14).

A serializer (1.25G Serdes) coupled to said data translation unit (codec 8B/10B) configured to receive said translated predetermined data and accordingly to generate a corresponding encoded data (at the receiving side, the 1.25G Serdes must convert the 10-bit parallel stream into an encoded 10-bit stream at a bit rate of a GbE signal, see col. 4, lines 38-44).

Regarding claims 58 and 65, it is inherent that in the receiving direction the 9-bit data entering the codec 8B/10B from MUX in Fig. 4 must have a data rate of 1,125 Mb/s since in the transmitting side the rate output at the output of the codec 22-1 in Fig. 2 is 1.125 Gb/s, see col. 4, lines 55-57.

Regarding claims 60-63 and 67-70, as illustrated in Fig. 4, Azizoglu teaches an apparatus comprising:

A demultiplexer (Deinterleaver receiving input data from SONET framer 36) configured to demultiplex received data, (at the receiving side, the received data is input into Deinterleaver inside Deinterleaver FPGA 64, col. 6, lines 4-12).

A data translation unit (codec 8B/10B 22-1) coupled to the demultiplexer (Deinterleaver) configured to translate the multiplexed data to a predetermined data which includes 10-bit data (codec 22-1 re-insert the run-length code to produce 10-bit parallel stream, col. 6, lines 12-14, see also col. 4, lines 39-44 and 47-51).

A serializer (1.25G Serdes) coupled to said data translation unit (codec 8B/10B) configured to receive said translated predetermined data and accordingly to generate a corresponding encoded data, wherein said serializer is configured to synchronize the translated predetermined data (at the receiving side, the 1.25G Serdes must convert and synchronize the 10-bit parallel stream into an encoded 10-bit stream at a bit rate of a GbE or 1.25Gb/s signal, see col. 4, lines 38-44).

13. Claims 51, 52, and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by Moshe et al. ("Moshe") (USPN 6,914,941 B1).

Regarding claims 51 and 53, as shown in Fig. 3, Moshe teaches an apparatus comprising:

A clock recovery unit (104) configured to received an encoded data (encoded data in the E3 signal) (col. 6, lines 5-8).

A data translation unit (114) coupled to said clock recovery unit (104), configured to translate said received data to a predetermined data, wherein said predetermined data includes a 9-bit data (Mux 114 adds framing bits to the received serial data output by FIFO 108 in order to obtain an effective data rate for 18 E1 signals of 35.568 Mbps, col. 6, lines 13-27, a 9-bit data is not defined, therefore reads on 9 bits data contained in the effective data rate of 35.568 Mbps).

An inverse multiplexer (102) coupled to said data translation unit, configured to inverse multiplex said translated predetermined data, wherein said inverse multiplexer is further configured to synchronize said multiplexed predetermined data (data input by Mux 114 into IMUX 102) to a predetermined clock signal (112), wherein said predetermined clock signal includes a phase locked loop clock signal (112) (IMUX 102 splits up the signal from MUX 114 into 18 individual E1 signals, col. 6, lines 8-13 and 27-32).

Regarding claim 52, it is inherent that said 9-bit data includes one of an arbitrary set of 9-bit data (col. 6, lines 13-27).

14. Claims 54 and 57 are rejected under 35 U.S.C. 102(e) as being anticipated by Arsenault et al. ("Arsenault") (USPN 6,728,966 B1).

Regarding claim 54, as shown in Fig. 2, Arsenault teaches an apparatus comprising:

A clock recovery unit (DEMOD 54) configured to receive an encoded data (encoded data is received at 54 and output into 56, col. 5, lines 57-58).

A data translation unit (56) coupled to said clock recovery unit, configured to translate said received data to a predetermined data (data is decoded by 56, col. 5, lines 57-58).

An inverse multiplexer (62) coupled to said data translation unit, configured to inverse multiplex said translated predetermined data (col. 6, lines 5-14).

A modem (86) coupled to said inverse multiplexer (62) configured to receive said inverse multiplexed translated predetermined data for transmission (col. 5, line 65).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 5, 9-11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stanger et al. ("Stanger") (USPN 6,097,435) in view of Moshe et al. ("Moshe") (USPN 6,914,941 B1).

Regarding claims 5 and 16, Stanger fails to teach that the clock delivery unit recovers a clock signal from the received encoded data.

However, in an analogous art as shown in Fig. 3, Moshe teaches a clock delivery unit (interface 104) recovers a clock signal from received encoded data (E3 signal), col. 6, lines 5-8.

Given the teaching of Moshe, it would have been obvious to one skilled in the art at the time the invention was made to modify the teaching of Stanger to include that the clock delivery unit recovers a clock signal from the received encoded data. The suggestion/motivation to do so would have been to keep the input data rate, i.e. line 32 in Fig. 4 of Stanger, constant throughtout the transmission path as suggested by Moshe (col. 6, lines 8-11).

Regarding claims 9-11, Stanger fails to explicitly teach that the inverse multiplexing includes synchronizing the inverse multiplexed predetermined data to a predetermined clock signal which includes a phase locked loop clock signal.

However, in an analogous art as shown in Fig. 3, Moshe teaches the inverse multiplexing (102) includes synchronizing the inverse multiplexed predetermined data to a predetermined clock signal which includes a phase locked loop clock signal (112), col. 6, lines 5-13 and 27-32.

Given the teaching of Moshe, it would have been obvious to one skilled in the art at the time the invention was made to modify the teaching of Stanger to include that the inverse multiplexing includes synchronizing the inverse multiplexed predetermined data to a predetermined clock signal which includes a phase locked loop clock signal. The suggestion/motivation to do so would have been to keep the input data rate, i.e. line 32 in Fig. 4 of Stanger, constant throughout the transmission path as suggested by Moshe (col. 6, lines 8-11).

17. Claims 27 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rowan et al. ("Rowan") (USPN 6,529,303 B1).

Regarding claims 27 and 39, Rowan fails to teach that the plurality of STS-3 signals includes eight STS-3 signals.

However, Rowan suggests that alternate embodiment can vary the number, bit rate, format, and protocol of some of these tributaries 160, col. 13, lines 35-43. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the number of STS-3 to any number including eight to produce the outgoing tributary with a higher speed signal/tributary as such modification involves only routine skill in the art.

Claims 59 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azizoglu et al. ("Azizoglu") (USPN 6,430,201 B1) in view of Smischny (USPN 5,166,890).

Regarding claims 59 and 66, Azizoglu does not teach that the multiplexer is further configured to perform parity checks on the received data. However, in an analogous art, Smischny teaches Mux 28 in Fig. 5 that performs parity checks on received data (col. 7, lines 16-18).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the teaching of Azizoglu to include that the multiplexer is further configured to perform parity checks on the received data. The suggestion/motivation to do so would have been to enable the multiplexer to produce a logic level output when a parity error is detected as taught by Smischny (col. 7, lines 16-18).

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nittaya Juntima whose telephone number is 571-272-3120. The examiner can normally be reached on Monday through Friday, 8:00 A.M - 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nittaya Juntima
December 1, 2005

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER